IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hitoshi IRINO

Title: SEMICONDUCTOR PROTECTION ELEMENT, SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

Appl. No.: 10/796,999

Filing Date: 3/11/2004

Examiner: Lee, Calvin

Art Unit: 2818

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith on Form PTO/SB/08 is a listing of a document known to Applicant in order to comply with Applicant's duty of disclosure pursuant to 37 CFR §1.56.

The submission of any document herewith, which is not a statutory bar, is not intended as an admission that such document constitutes prior art against the claims of the present application or that such document is considered material to patentability as defined in 37 CFR §1.56(b). Applicant does not waive any rights to take any action which would be appropriate to antedate or otherwise remove as a competent reference any document which is determined to be a *prima facie* art reference against the claims of the present application.

TIMING OF THE DISCLOSURE

The listed documents are being submitted in compliance with 37 CFR §1.97 after filing a Request for Continued Examination.

RELEVANCE OF EACH DOCUMENT

All of the documents are in English. The documents were cited in a South Korean Office Action that issued December 21, 2005 in a counterpart South Korean application.

As a statement of relevance, a translation of a portion of the South Korean Office Action that issued December 21, 2005 with respect to a counterpart South Korean patent application is provided below.

1. The content of the inventions described in Claims 1 through 16 and 26 through 41 of the present invention is that they provide a semiconductor substrate with a first region having a first impurity concentration and a pair of second regions having a second impurity concentration greater than the impurity concentration of the first region, with a silicide layer being applied so as to touch the surface of the second regions, the first region having a first surface region not covered by the silicide layer and the second regions having a second surface region not covered by the silicide layer, the silicide layers being formed so that the second surface regions are continuous with the first surface region and so that the second surface regions

are exposed, with the silicide layers being low resistance regions with a relative low resistance, the second surface layers being intermediate resistance regions with an intermediate resistance, and the first surface region being a high resistance region with a relatively high resistance, whereby the occurrence of electrostatic discharge does not lead to heat concentration in the high resistance region. However, Cited Invention 1 (U.S. Patent No. 6,531,745 (03/11/2003)) presents content to the effect that protection against electrostatic discharge is obtained by an arrangement whereby a first and second n-layer region are formed, with a gate dielectric layer being formed in the n-type region and a polysilicon gate being formed in the gate induction layer, such that resistor conductivity is amplified by a bias function impressed on the polysilicon gate.

2. Furthermore, the inventions described in Claims 17 through 25 and 42 through 56 relate to a manufacturing method based on the same technical idea as the inventions described in Claims 1 through 16 and 26 through 41. Cited Invention 2 (U.S. Patent No. 6,528,380 (03/04/2003)) relates to a method of forming a resistor on a substrate, presenting content to the effect that protection from electrostatic discharge is obtained by

an arrangement wherein an n-type drain is formed in an n-type silicon region, an n-type source region is formed in an n-type silicon region, a dielectric layer is formed over the n-type silicon region, a polysilicon gate is formed over the dielectric layer, and the conductivity of the resistor is amplified by adjusting the gate bias function for the polysilicon gate, and the drain region is short circuited in order to prevent potential difference affecting the dielectric layer when a high voltage is impressed onto the drain region. The present inventions are similar in arrangement when compared to Cited Invention 1 and Cited Invention 2, and are in the same category in terms of effect. Thus, the present inventions could be easily invented by a person having ordinary knowledge in this technical field based on Cited Invention 1 and Cited Invention 2.

Applicant's statements regarding the South Korean Office Action are based on a partial translation that Applicant's representative obtained. These statements should in no way be considered as an agreement by Applicant with, or an admission of, what is asserted in the South Korean Office Action.

Applicant respectfully requests that each listed document be considered by the Examiner and be made of record in the present application and that an initialed copy of Form PTO/SB/08 be returned in accordance with MPEP §609.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 CFR §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

Respectfully submitted,

Date January 30, 2006 By _____

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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: January 30, 2006

(use as many sheets as necessary)

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Complete if Known	
Application Number	10/796,999
Filing Date	3/11/2004
First Named Inventor	Hitoshi IRINO
Group Art Unit	2818
Examiner Name	Lee, Calvin
Attorney Docket Number	045054-0158

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	U.S. Patent Document Kind Code[2] (*if known*)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		6,531,745	B1	Woolery et al.	03-11-2003	
		6,528,380	B2	Woolery et al.	03-04-2003	

U.S. PATENT APPLICATION DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Application Document Serial Number	U.S. Patent Application Document Kind Code[2] (*if known*)	Name of Patentee or Applicant of Cited Document	Filing Date of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (*if known*)	Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[6]

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2]See attached Kinds of U.S. Patent Documents. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

Burden Hour Statement: This form is estimated to take 2.0 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.